In Paragraphs [0027] to [0030], please amend the paragraphs as follows:

[0024] As shown in FIG. 1 and 2, the clock signal detector 10 can be connected to the path of clock signal transmission, and the data signal detector 20 can be connected to the path of data signal transmission. The clock signal detector 10 ~~is design with~~ has the following components: ~~(as shown in FIG. 2, 3, and 4).~~

[0025] As shown in FIGS. 2-4, the clock signal detector 10 includes a ~~A~~ signal converter 11, which is the signal converter U1 between the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal input end and Low-Voltage Transistor-Transistor Logic (LVTTL) output end to convert coupled input differential clock signal into single input clock signal.

[0026] ~~A~~ There is also a rectifying-filtering circuit 12, which can be a stand-alone rectifying component (i.e. micro inductor L1) connected to the signal converter 11. It transforms the clock signal inputted from the signal converter into D.C. potential signal output.

[0027] ~~An~~ The present invention also includes an inverter 13, which is connected to the rectifying-filtering circuit 12 - It serves as a buffer for Inductor L1. At the input end, the regularly present D.C. potential signal is inputted into the base of Transistor Q3, the transistor Q3 will get into the status of "ON". Thus, the collector of the transistor Q3 regularly outputs a low potential signal. Conversely, when the clock signal disappears, in other words, no signal is inputted into the base of transistor Q3' and the transistor Q3 will get into the status of cut-off. Thus the collector of the transistor Q3 regularly outputs a high potential signal. Based on the above description, this mechanism achieves the effect of inversion, and the signal outputted is the ~~said~~ clock signal transmission abnormality detection potential signal, which is the resulted potential signal output, reversed from the D.C. potential signal inputted from the rectifying-filtering circuit 12.

In Paragraphs [0029] to [0033], please amend the paragraphs as follows:

[0029] Furthermore, as shown in FIG. 2, 5, and 6, ~~the~~ there is a data signal detector 20 ~~contains:~~.

[0030] ~~A~~ The data signal detector 20 includes a signal converter 21, which acts as the Signal Converter U1 between the Low-Voltage Positive Emitter Coupling Logic (LVPECL) signal input end and the output end of a set of Low-Voltage Transistor-Transistor Logic (LVTTL) signal. This converter converts coupled input differential data signal into single output data signal.

[0031] ~~An~~ There is also an Integral Charger 22, which is connected to the signal converter 21, as shown in FIGS. 7 and 8. The second resister R2 of the integral charger is connected to the capacitor C2 in parallel, which is then connected to the first resister R1 with a tandem connection. In which, the first resistor R1 is the input end and the tandem connection point between the first resistor R1 and the second resistor R2 is the output end. The other end of the second resistor R2 is grounded, which also converts the data signal, inputted from the signal converter 21, into a pulse type integral potential signal and outputs it to the next stage. This potential signal approximately corresponds to a constant ratio of positive potential signal pulse.

[0032] ~~An~~ The present invention also has an Inverter 23, which is connected to the integral charger 22; it serves as the Logic Gate U2 and makes logic decisions to the inputted integral potential signal. It decides the status of inverting by a internal threshold voltage which is setting in logic IC. If the data ratio of positive potential signal in the differential data signal is transmitted normally, in other